IN THE SPECIFICATION

Please amend the paragraph in the specification beginning on page 5 at line 13 as follows:

~~FIGs. 11A-11B illustrate an example cell/packet processor of the Receiver FIFO Hardware Assist (HWA) mechanism according different embodiments of the present invention;~~

FIG. 11 illustrates an example header checking process without using the Receiver FIFO Hardware Assist (HWA) mechanism according to an embodiment of the present invention;

Please amend the paragraph in the specification beginning on page 5 at line 15 as follows:

~~FIGs. 12A-12B illustrate example header comparators of the Receiver FIFO Hardware Assist (HWA) mechanism according different embodiments of the present invention;~~

FIG. 12 illustrates an example header checking process using the Receiver FIFO Hardware Assist (HWA) mechanism;

Please amend the paragraph in the specification beginning on page 5 at line 17 as follows:

~~FIG. 13 illustrates an example header checking process without using the Receiver FIFO Hardware Assist (HWA) mechanism according to an embodiment of the present invention;~~

FIGs. 13A-13B illustrate different embodiments of an example cell/packet processor of the Receiver FIFO Hardware Assist (HWA) mechanism;

Please amend the paragraph in the specification beginning on page 5 at line 19 as follows:

~~FIG. 14 illustrates an example header checking process using the Receiver FIFO Hardware Assist (HWA) mechanism according to an embodiment of the present invention;~~

FIGs. 14A-14B illustrate example implementations of header comparators of the cell/packet processor;

Please amend the paragraph in the specification beginning on page 50 at line 21 as follows:

As described with reference to FIGs. ~~10, 11A-11B, 12A-12B and 14~~ 10, 12, 13A, 13B, 14A, and 14B, the Receiver FIFO Hardware Assist (HWA) mechanism according to an embodiment of the present invention has a low gate count and is expandable as well as scalable. All header checks and comparisons are implemented in hardware and performed in parallel with each other while offloading the Micro-Engine (ME) 710 from having to spend considerable clocks to process the cell/packet header. This allows the Micro-Engine (ME) 710 to do other work while header checks are being completed. As a result, ME performance can be enhanced and latency can be decreased significantly.